

CLOCK SIGNAL DUTY CYCLE ADJUST CIRCUIT

Abstract

Systems and methods for independently adjusting a duty cycle of an input clock
5 signal in an IC to compensate for uncertainties and distortions in the logic signals
resulting from the logic signals propagating through the IC to improve system
performance. This is accomplished by inputting first and second programming
instructions into one of a plurality of edge-triggered circuits to select one of a series of
plurality of incremental or decremental duty cycle adjust circuits to adjust the duty cycle
10 of a clock signal as a function of the first and second programming instructions.

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